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Claims

[c1] 1.A semiconductor structure comprising:
a substrate comprising a plurality of levels formed thereupon;
a metal-insulator-metal (MIM) capacitor formed on an inter-level dielectric layer
in a first of the plurality of levels; and
an insulator layer selectively formed on said MIM capacitor, wherein portions of
the inter-level dielectric layer are insulator layer-free.

[c2] 2.The semiconductor structure of claim 1, wherein said MIM capacitor comprises a bottom metal plate formed on the inter-level dielectric layer, a capacitor dielectric layer on the bottom metal plate and a top plate on the capacitor dielectric layer.

[c3] 3.The semiconductor structure of claim 2, wherein said insulator layer encapsulates the top metal plate and the capacitor dielectric layer.

[c4] 4.The semiconductor structure of claim 2, wherein edge portions of said insulator layer are
self-aligned to respective edge portions of the bottom

metal plate.

[c5] 5.The semiconductor structure of claim 1, wherein said insulator layer comprises silicon nitride.

[c6] 6.The semiconductor structure of claim 1, wherein the inter-level dielectric layer comprises silicon oxide.

[c7] 7. The semiconductor structure of claim 1, wherein a second of the plurality of levels is located between an upper surface of the substrate and the first of the plurality of levels, the second of the plurality of levels comprises a field effect transistor (FET) formed thereupon.

[c8] 8.The semiconductor structure of claim 7, wherein said portions provide a path for diffusion of hydrogen and/or deuterium to the FET.

[c9] 9. A method of forming a semiconductor structure comprising the steps of:
providing a substrate comprising a plurality of levels formed thereupon;
forming a metal-insulator-metal (MIM) capacitor on an inter-level dielectric layer
in a first of the plurality of levels; and
selectively forming an insulator layer on said MIM capacitor, wherein portions of

the inter-level dielectric layer are insulator layer-free.

[c10] 10.The method of claim 9, wherein said MIM capacitor comprises a bottom metal plate adjacent the inter-level dielectric layer, a capacitor dielectric layer on the bottom metal plate and a top plate on the capacitor dielectric layer.

[c11] 11. The method of claim 9, wherein said step of selectively forming comprises:
forming said insulator layer on said MIM capacitor and exposed portions of
the inter-level dielectric layer;
patterning a masking layer on said insulator layer; and
removing exposed portions of said insulator layer to form said insulator layer-
free portions.

[c12] 12. The method of claim 11, wherein said step of forming said insulator layer comprises
chemical vapor deposition.

[c13] 13. The method of claim 11, wherein said removing step comprises reactive ion etching.

[c14] 14.The method of claim 11, wherein said removing step further comprises removing
portions of the bottom metal plate.

[c15] 15.The method of claim 14, wherein edge portions of said insulator layer are
self-aligned to respective edge portions of the bottom metal plate.

[c16] 16. The method of claim 9, wherein said insulator layer encapsulates the top metal plate and the capacitor dielectric layer.

[c17] 17.The method of claim 9, wherein said insulator layer comprises silicon nitride.

[c18] 18.The method of claim 9, wherein the inter-level dielectric layer comprises silicon oxide.

[c19] 19. The method of claim 9, wherein a second of the plurality of levels is located between an upper surface of the substrate and the first of the plurality of levels, the second of the plurality of levels comprises a field effect transistor (FET) formed thereupon, and said portions provide a path for diffusion of hydrogen and/or deuterium to the FET.

[c20] 20.An integrated circuit comprising:
a substrate comprising a lower level including a plurality of field effect
transistors and an upper level;

a metal-insulator-metal (MIM) capacitor formed on an inter-level dielectric layer
in the upper level; and
a silicon nitride layer selectively encapsulating a portion of the MIM capacitor, wherein portions of the inter-level dielectric layer are silicon nitride layer-free, said silicon nitride layer-free portions allow hydrogen and/or deuterium to diffuse to the FETs.

[c21] 21.The integrated circuit of claim 20, wherein the MIM capacitor comprises a bottom metal plate adjacent the inter-level dielectric layer, a capacitor dielectric layer on the bottom metal plate and a top plate on the capacitor dielectric layer.

[c22] 22.The integrated circuit of claim 21, wherein said silicon nitride layer encapsulates the top
metal plate.

[c23] 23.The integrated circuit of claim 22, wherein said silicon nitride layer encapsulates the capacitor dielectric layer.

[c24] 24.The integrated circuit of claim 23, wherein said silicon nitride layer encapsulates a portion of the bottom metal plate.